

	L #	Hit	S arch T xt	DB
1	L1	1933	(361/748,792,795,803).ccls.	USP AT; US-P GPU B
2	L2	1913	(174/255,258,259).ccls.	USP AT; US-P GPU B
3	L3	1895	(29/830,846).ccls.	USP AT; US-P GPU B
4	L4	1453	(228/180.21,180.22).ccls.	USP AT; US-P GPU B
5	L5	3393	(428/209,901).ccls.	USP AT; US-P GPU B
6	L6	9231	1 2 3 4 5	USP AT; US-P GPU B
7	L7	2317	6 and @pd>=20010401	USP AT; US-P GPU B

	L #	Hit	S arch T xt	DB
8	L8	1029	7 and adhesive\$2	USP AT; US-P GPU B
9	L9	952	8 and (layer\$2 laminat\$3)	USP AT; US-P GPU B
10	L10	756	9 and (mill\$3 ablati\$2 grind\$3 remov\$3)	USP AT; US-P GPU B
11	L11	735	10 and ((printed adj circuit\$1) board\$1 substrate\$1)	USP AT; US-P GPU B
12	L12	12	("4148844" "4353954" "4769270" "5492863" "5674343" "5777386" "5821628" "5830949" "5859170" "5916675" "6008311" "6023096").PN.	USP AT
13	L13	4	("4816323" "5346750" "5766670" "6010768").PN.	USP AT
14	L14	14	("3795047" "4648179" "5252519" "5374469" "5444189" "5744758" "5768108" "5822856" "5876842" "6159586" "6217987" "6237218" "6242079" "6248428").PN.	USP AT

	L #	Hit	S arch T xt	DB
15	L15	4	("4299873" "4712161" "5374469" "5652042").PN.	USP AT
16	L16	25	("3356624" "4504607" "4510276" "4615950" "4713298" "4750976" "4752499" "4820549" "4888269" "4902726" "4948700" "4990395" "5009982" "5021472" "5055321" "5055378" "5061744" "5137936" "5175060" "5302492" "5519177" "5532094" "5741575" "5753722" "5948514").PN.	USP AT
17	L17	21	10 not 11	USP AT; US-P GPU B
18	L18	196	9 not 10	USP AT; US-P GPU B
19	L19	77	8 not 9	USP AT; US-P GPU B